REMARKS

Applicants have amended their specification in light of objections to the specification and drawings set forth in Items 2 and 3 on pages 2 and 3 of the Office Action mailed April 14, 2008, and in order to correct the spelling of "polyimide" and correct other typographical errors. Specifically, on page 2 of Applicants' specification, the heater has been designated by reference character "140", consistent with Fig. 1(c) of Applicants' original disclosure; and page 2 of Applicants' specification has been further amended to delete the reference character "600" with respect to the thermoset resin as described on page 2, line 22, of Applicants' specification. It is respectfully submitted that these amendments to the specification do not add new matter to the application.

Applicants have amended Fig. 1 to designate this figure by the legend "BACKGROUND ART". In light thereof, the objection to the drawings as set forth in Item 3a on page 2 of the Office Action mailed April 14, 2008, is moot.

Applicants have amended Fig. 2(b) to delete the reference character "11", and the lead line therefor. AS indicted previously, Applicants have amended their specification to delete the reference character 600 at page 2, line 22. In light of these amendments respectively to Fig. 2(b) and to page 2, line 22, it is respectfully submitted that the bases for objection to the drawings as set forth in Item 3b on page 2 of the Office Action mailed April 14, 2008, is moot.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have cancelled original claims 1-17 without prejudice or disclaimer, and are adding new claims 18-34 to the application. Of these newly added claims, claim 18 is the sole newly added independent claim, and claims 18-33 correspond respectively to original claims 1-13

and 15-17, respectively, with amendments to original claims as discussed in the following.

Thus, claim 18, recites that the electronic device manufactured has IC elements, with each IC element having electrodes formed respectively on the respective surfaces of a pair of opposed sides thereof, the electronic device also having first and second circuit layers. Claim 18 further defines a step of forming a slit in the first or second circuit layer; and recites a step of forming (a) a first connecting part for electrically connecting the electrode of one side of the IC elements and the first circuit layer, on the one side, (b) a second connecting part for electrically connecting the electrode of the other side of the IC elements and the second circuit layer, and a third connecting part for electrically connecting the first and second circuit layers so that the second connecting part and the third connecting part are connected spanning the slit. Claim 18, as compared with original claim 1, also recites that the step of positionally aligning is performed while continuously supplying the IC elements "individually into an IC elements transport mechanism".

Claim 19, as compared with original claim 2, recites that the IC element is delivered by running the IC element holding part of the transport mechanism. Claims 20 and 21, as compared with previously considered claims 3 and 4, recite that the step of continuously supplying the IC elements includes a step of individually holding an IC element in an IC element holding part of a IC elements transport mechanism having not less than one IC elements holding part, and a step of delivering the IC element thus held by running the IC element holding part of the transport mechanism. Claim 20 additionally recites that the IC elements transport mechanism is disc shaped; and claim 21 additionally recites that the IC element holding part is formed as a notch shape.

Claims 22-24, as compared with claims 5-7, respectively, further define the step of continuously supplying the IC elements as including a step of aligning the IC elements by action of an IC elements alignment/supply mechanism to facilitate individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part, and a step of delivering the IC element thus held by running the IC element holding part of the transport mechanism. Claim 23 further recites that the IC elements alignment/supply mechanism is a line feeder, and claim 24 further recites that the IC elements alignment/supply mechanism is a high frequency alignment feeder.

Attention is also directed to claim 34, reciting that the electrical connections of electrodes of the IC elements and the circuit layers are made via first and second anisotropic conductive adhesive layers, with a total thickness of the first and second anisotropic conductive adhesive layers being not less than half the thickness of the IC elements.

In connection with claim 34, note, for example, page 14, lines 16-19 of Applicants' specification. In connection with the other newly added claims (claims 18-33), note, for example, Figs. 2(a) and 2(b), as well as Figs. 3 and 4; and note also descriptions on pages 3, 4, 5, 9, 16, 17, 23, 27 and 28, of Applicants' specification.

The objection to claim 2 as set forth in Item 4a on page 3 of the Office Action mailed April 14, 2008, is moot insofar as applicable to present claim 19, reciting the IC element holding part of the transport mechanism.

Applicants respectfully traverse the objection to previously considered claims 3-7, set forth in Item 4b on pages 3 and 4 of the Office Action mailed April 14, 2008, particularly insofar as applicable to present claims 20-24. Contrary to the

contention by the Examiner, it is respectfully submitted that the previously considered claims further limited the process, in limiting the apparatus used therein. That is, while parent claims could use any apparatus for practicing the recited steps, claims 3-7 further define the process by reciting the apparatus in which the processing steps take place. In any event, claims 20-24 recite steps, which are sub-steps of the step of continuously supplying the IC elements. In light of the specific steps in claims 20-24, the previously objection to claims 3-7 is moot insofar as applicable to claims 20-24. Claim 28 recites that "the gaps between the first and second circuit layers are sealed by the thermal compression", thus avoiding the basis for the objection set forth in Item 4c on page 4 of the Office Action mailed April 14, 2008. Claim 31, as compared with claim 15, recites that the first and second circuit layers include aluminum; accordingly, the contention by the Examiner, in connection with previously considered claim 15, that "the conductive layer" lacks antecedent basis, is moot. Objections to claims 16 and 17 as set forth in Item 4e on page 4 of the Office Action mailed April 14, 2008, are moot, in light of claims 32 and 33 presently in the application.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed April 14, 2008, that is, the teachings of the U.S. patent documents to Aoyama, et al., Patent No. 7,278,203, to Keen, et al., Patent No. 6,732,498, to Moskowitz, et al., Patent No. 5,528,222, to Usami, Patent Application Publication No. 2001/0012645, and to Green, et al., Patent Application Publication No. 2003/0136503, under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither disclosed nor would have suggested such a manufacturing method for an electronic device having IC elements with electrodes formed respectively on opposed sides thereof, the device also having first and second circuit layers, wherein the method includes, inter alia, forming a slit in the first circuit layer or the second circuit layer; and forming first through third connecting parts respectively (i) for electrically connecting the electrode of one side of the IC elements and the first circuit layer, on the one side, (ii) for electrically connecting the electrode of the other side of the IC elements and the second circuit layer, and (iii) for electrically connecting the first and second circuit layers so that the second connecting part and the third connecting part are connected spanning the aforementioned slit; and wherein the step of positionally aligning the connection surfaces is performed while continuously supplying the IC elements individually into an IC elements transport mechanism. See claim 18.

Furthermore, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of individually holding an IC element in an IC element holding part of a transport mechanism, as in claims 19-21, and, in particular, wherein the transport mechanism is a disc shaped IC elements transport mechanism (see claim 20), or wherein the IC element holding part is formed as a notch shape (see claim 21).

In addition, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as

in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of aligning the IC elements by action of an IC elements alignment/supply mechanism to facilitate individually holding an IC element in the holding part, with a step of delivering the element held by such holding part by running the IC element holding part of the transport mechanism (note claims 22-24), in particular, wherein the IC elements alignment/supply mechanism is a line feeder (see claim 23) or is a high frequency alignment feeder (see claim 24).

Moreover, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, having further features as in the remaining dependent claims, including (but not limited to) wherein the electrical connection of an electrode and at least one of the circuit layers is made via an anisotropic conductive adhesive layer (see claim 25); and/or wherein the method further includes connecting at once, the electrodes of the IC elements and at least one layer from among the first and second circuit layers, with the step of connecting being performed after the step of positionally aligning the connection surfaces (see claim 26), in particular, wherein the electrode of the IC elements and the at least one layer from among the first and second circuit layers are connected by thermal compression (see claim 27), with gaps between the first and second circuit layers being sealed by the thermal compression (see claim 28); and/or wherein the method further includes a step of cutting a continuum of the plurality of IC elements into individual pieces, with the step of cutting being performed after the connecting step (see claim 29); and/or wherein a conductive layer is formed on the surface of at least

one from among the first and second circuit layers (see claim 30); and/or wherein the first and second circuit layers include aluminum (see claim 31); and/or base substrate material supporting at least one of the first and second circuit layers, as in claims 32 and 33; and/or thickness of the anisotropic conductive adhesive layers, as in claim 34.

The present invention is directed to a method of manufacturing an electronic device, illustrated (but not limited to) by a noncontact type individual identification device having IC elements.

In recent years, individual identification systems that employ radio frequency identification tags have been considered; such systems include an external antenna attached to IC elements, which enables communication to be performed over several meters. One type of such system is a TCP (Tape Carrier Package) inlet, employing a tape automated bonding method in which IC elements having all external electrodes formed on the same surface thereof are mounted, each individually, on a tape carrier formed of a polyimide substrate.

As described in the first full paragraph on page 3 of Applicants' specification, other inlet structures include IC elements in which the external electrodes of the IC elements are formed individually on both of a pair of opposite surfaces of the IC element. The IC elements in the proposed structure have, respectively, two external electrodes formed individually on the surfaces of the IC elements, and are furnished with an excitation slit type dipole antenna, the external electrodes formed individually on each of the surfaces of the IC elements being disposed between the legs of an antenna to manufacture a sandwich antenna construction.

However, various problems arise in connection with previously proposed inlet structures and methods of manufacture thereof, as described on pages 4 and 5 of

Applicants' specification. Thus, it is still desired to provide a manufacturing method for manufacturing a semiconductor device which can be utilized in an identification system, which can manufacture the device at low cost and with superior productivity, and wherein the device has satisfactory communication properties.

Against this background, Applicants achieve the foregoing objectives by the present method, including, inter alia, wherein each IC element has electrodes formed respectively on the respective surfaces of a pair of opposed sides of the IC element, with a slit being formed in the first or second circuit layer, with connecting parts electrically connecting the respective electrodes with the first and second circuit layers, and with the first and second circuit layers being connected so that the second and third connecting parts are connected spanning the slit, the IC elements individually being continuously supplied into an IC elements transport mechanism in positionally aligning the connection surfaces of the IC elements and one of the first and second circuit layers.

By continuously supplying the IC elements individually into an IC elements transport mechanism as in the present claims, in particular, into a notch at the periphery of a disc shaped transport mechanism, a plurality of IC elements up to a maximum number equivalent to the number of, e.g., notches, can be simultaneously delivered, even when the delivered IC elements are arranged individually on the second circuit layer and the antenna circuits, so that superior productivity can be realized in comparison to the case where the IC elements are held by suction using a vacuum suction device or the like, and delivered and arranged one by one. As increased productivity is realized, available operating time per inlet device is reduced. Note the first full paragraph on page 16 of Applicants' specification.

By forming the connecting structure (that is, the first through third connecting parts, particularly the second and third connecting parts) spanning the slit, high precision positional alignment of the external electrode on that surface of the IC elements that is on the side in contact with the antenna circuit, with the excitation slit on the antenna circuit, is not necessary, thus reducing costs associated with manufacturing equipment and facilitating high-speed delivery of the IC elements. See page 16, lines 13-18, of Applicants' specification.

By providing electrical connections of the electrodes with the first and second circuit layers via an anisotropic conductive adhesive layer, as in, for example, claim 25, it is not necessary to have a surface coating over the antenna circuits, and there is no need to use a highly heat resistant base substrate, making it possible to use an inexpensive base material and antenna circuit, thereby enabling cost reductions. Note the paragraph bridging pages 16 and 17 of Applicants' specification.

In addition, as the IC elements are accommodated individually, e.g., in notches in the IC elements transport mechanism, with a plurality of notches arranged circumferentially around the outside of a disc shaped transport mechanism, a maximum number of IC elements equivalent to the number of notches can be simultaneously delivered, providing improvement in the productivity. Note the last full paragraph on page 18 of Applicants' specification.

Aoyama, et al. discloses a transfer apparatus for transferring parts onto works with revolving end-effectors, the apparatus being contemplated as used as a chip transfer apparatus for transferring chips onto works, as described most generally in column 2, lines 8-31 of this patent. Note also column 3, lines 55-67; and column 4, lines 35-48, of Aoyama, et al., as well as Fig. 1, describing transfer apparatus 1

including a first carrier 3, a second carrier 5 and two transfer engines 6, with the second carrier 5 carrying works 4 onto which chips 2 can be transferred, the first carrier 3 carrying chips 2 on it and feeding the carried chips. See also column 5, lines 17-21, describing, in connection with Fig. 1, that the chip feeder 30 takes the form of a roller, around which a tape may temporarily retain chips 2 on it until they are fed; or that, alternatively, a continuous material might be fed and cut into chips, which might then be fed to the chip feeder 30.

It is respectfully submitted that Aoyama, et al. discloses a method of transferring chips, wherein the chips have all electrodes on one side of the IC element. It is emphasized that Aoyama, et al. discloses an IC element having left-side and right-side faces, and does not disclose, nor would have suggested, and in fact would have taught away from, structure wherein the IC element is sandwiched by external electrodes respectively on opposite sides of the IC element.

Furthermore, it is respectfully submitted that Aoyama, et al. does not disclose formation of a slit at as in the present claims, or formation of the first through third connecting parts, with the second and third connecting parts being connected spanning the slit, and advantages achieved by the present invention due to the recited processing.

It is respectfully submitted that the presently claimed method, including formation of the connecting parts such that the second and third connecting parts being connected spanning the slit, eliminates the need for high precision processing between the respective electrodes, thereby enabling reduction in equipment and price of production facilities, reducing production costs, while increasing speed of production. In this regard, it is respectfully submitted that according to the present invention, with structure being formed with a configuration as in the present claims,

accuracy of mounting need only be within 0.3 mm of the prescribed position. In contrast, Aoyama, et al. needs a high precision positioning between external electrodes and antenna terminals, because all electrodes are formed on a same face of an IC element. Note that Aoyama, et al. discloses necessary accuracy in positioning of "tens of microns and some microns in accuracy, thereby improving the productivity and the mounting quality". Such accuracy of "tens of microns and some microns" is clearly a much more difficult assignment than an accuracy within 0.3 mm, as satisfactory with the present invention.

Moreover, it is respectfully submitted that Aoyama, et al. discloses that the chips are provided on a tape that temporarily retains the chips until they are fed. Such disclosure in Aoyama, et al. would have taught away from the presently claimed invention, including wherein the IC elements are individually supplied into the IC elements transport mechanism.

It is respectfully submitted that the teachings of the additional references applied by the Examiner would not have rectified the deficiencies of Aoyama, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Keen, et al. discloses apparatuses and methods for counting objects in a packaging product line, e.g., a piece count and collation system for controlled blending and distributing of confectionary objects (candies) wrapped by a flow-wrap apparatus. The methods are described most generally in column 2, lines 1-16, and include receiving a plurality of sequentially spaced objects partially wrapped by tube-wrapping, grasping each of the plurality of objects individually by a vacuum assisted grasping member, cutting and bonding ends of each individual partially wrapped object with a cut-and-seal apparatus, transferring the fully wrapped object to a

conveyor, and conveying the fully wrapped object away from the cut-and-seal device. See also column 1, lines 38-67 of Keen, et al.

Initially, it is respectfully submitted that the teachings of Keen, et al. would not have been properly combinable with the teachings of Aoyama, et al. Noting that Aoyama, et al. is directed to chip transfer apparatus, while Keen, et al. is directed to a system for piece counting and collation, e.g., of candy; and noting differences in problems addressed by Aoyama, et al. and by Keen, et al., it is respectfully submitted that one of ordinary skill in the art concerned with in Aoyama, et al. would not have looked to the teachings of Keen, et al. In other words, these two patents are directed to non-analogous arts.

Again emphasizing the differences in technologies in Aoyama, et al. and in Keen, et al., as well as differences in problems addressed, it is respectfully submitted that there would have been no reason to combine the teachings of Aoyama, et al. and of Keen, et al., as applied by the Examiner. Of course, without such reason for combining teachings, such combination of teachings is improper.

Even assuming, arguendo, that the teachings of Aoyama, et al. and of Keen, et al. were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including features as discussed previously in connection with claim 18, or the notch-shaped structure as in claim 20. In this regard, it is noted that Keen, et al. discloses a disc with notches; however, it is respectfully submitted that the holding part is not formed as a notch shape, but rather the holding part in Keen, et al. is the vacuum head 12. Such disclosure would have taught away from the present invention, including the IC element holding part which is formed as a notch, and advantages thereof.

In connection with claim 10, Moskowitz, et al. discloses a radio frequency circuit and memory in a thin flexible package, used as a radio frequency tag, the tag including a semiconductor circuit that has logic, memory and radio frequency circuits, the semiconductor being mounted on a substrate and being capable of receiving a RF signal through an antenna that is electrically connected to the semiconductor through connections on the semiconductor, the elements of the package being placed adjacent to one another, i.e., they are not stacked. Note column 3, lines 9-19. See also the paragraph bridging columns 3 and 4. This patent discloses a flexible covering material for the package, wherein a single layer of laminate such as polyethylene, polyester, mylar or polyimide may be used for covering. Note column 4, lines 49-60.

Even assuming, arguendo, that the teachings of Aoyama, et al. and of Moskowitz, et al. were properly combinable, such combined teachings would have neither taught nor would have suggested the aspects of the present invention including wherein each IC element has electrodes formed respectively on surfaces of a pair opposed sides of the element; and/or wherein the method includes forming a slit in the first or second circuit layer; and/or forming connecting parts as in the present claims, including forming the second and third connecting parts connected spanning the slit; and/or wherein positional alignment is performed while continuously supplying the IC elements individually into an IC elements transport mechanism, as in all of the present claims, and advantages thereof as discussed previously.

In connection with claims 11 and 15, Usami discloses a manufacturing method applicable to a non-contact type identification device particularly utilizing a thin semiconductor chip, the manufacturing method being described, for example, in

paragraphs [0005]-[0008] on page 1 of this patent document. See also paragraph [0049] on page 4 thereof.

Even assuming, arguendo, that the teachings of Usami were properly combinable with the teachings of Moskowitz, et al. and of Aoyama, et al., as applied by the Examiner, such combined teachings would have neither disclosed nor would have suggested features of the present invention as discussed previously, including, inter alia, forming the slit, or forming the connecting parts, including wherein the second and third connecting parts span the slit, and advantages thereof, as discussed previously, and/or individual supply of IC elements, as discussed previously, and advantages thereof.

Green, et al. discloses a method of manufacturing radio frequency identification tags and labels, the method being described, for example, in paragraph [0018] on page 2 of this patent publication. Note also paragraphs [0015], [0021] and [0022] of this publication.

Even assuming, arguendo, that the teachings of Green, et al. were properly combinable with the teachings of Aoyama, et al., Moskowitz, et al. and Usami, as applied by the Examiner in Items 16 and 17 on pages 12-14 of the Office Action mailed April 14, 2008, such combined teachings would have neither disclosed nor would have suggested the method as in the present claims, including, inter alia, the formation of the slit and/or forming of the connecting parts, particularly the second and third connecting parts which span the slit, or individual supply of IC elements, as in the present claims, and advantages thereof.

Furthermore, and again noting features of the present invention set forth in the dependent claims, referred to previously, it is respectfully submitted that any combination of teachings of references as applied by the Examiner would have

neither disclosed nor would have suggested such features in the dependent claims, in combination with features as in claim 18, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently pending in the above-identified application are respectfully requested.

To the extent necessary, Applicants hereby petition for an extension of time under 37 CFR 1.136. Kindly charge any shortage of fees due in connection with the filing of this paper, including any extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (case 1204.46401X00), and please credit any overpayments to such Deposit Account.

Respectfully submitted,

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